REMARKS

Prior to the present amendment, claims 1-7, 9, 11, 13, 20-23 and 30-35 were pending in the present application, claims 8, 10, 12, 14-19, and 24-29 having been canceled by previous amendment. By the present amendment and response, Applicant has amended claim 30. Thus, claims 1-7, 9, 11, 13, 20-23, and 30-35 remain pending in the present application. Applicant respectfully requests reconsideration and allowance of claims 1-7, 9, 11, 13, 20-23 and 30-35 in view of the above amendment and the following remarks.

A. Rejection of Claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9, 11, 13, and 20-23 under 35 USC §103(a) as being unpatentable over United States Patent Number 6,740,952 B2 to Fujishima et al. (hereinafter "Fujishima") in view of United States Patent Number 6,525,390 B2 to Tada et al. (hereinafter "Tada"), United States Patent Number 6,639,277 B2 to Rumennik et al. (hereinafter "Rumennik"), *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, 2000, Mc-Graw Hill, New York, 4th Edition, pp. 382,511, by Peter Van Zant (hereinafter "Van Zant"), *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, 1994, John Wiley & Sons, Inc., New York, 2nd Edition, pages 258-259, by Sorab K. Ghandhi (hereinafter "Ghandhi"), United States Patent Number 6,617,652 B2 to Masaaki Noda (hereinafter "Noda"); and United States Patent Number 5,801,431 to Niraj Ranjan (hereinafter "Ranjan"). For the reasons discussed below, Applicant respectfully submits

that the present invention, as defined by independent claim 1, is patentably distinguishable over Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan, either singly or in any combination thereof.

Independent claim 1 recites a semiconductor device with a novel field plate structure. The field plate structure is disposed over a reduced surface field ("resurf") region on the device and includes a first field plate disposed over a first insulation layer of a first thickness extending from said gate insulation layer. *See* claim 1 above. The field plate structure further includes a second field plate disposed over a second insulation layer of a second thickness, where the second insulation layer is formed over the first insulation layer. *Id.* The field plate structure also includes a third field plate spaced from the second field plate by a third insulation layer of a third thickness, where the first field plate includes a first portion spaced from a second portion by a first gap, and the first portion of the first field plate extends from the gate electrode. *Id.*

In claim 1, the second portion of the first field plate is electrically connected to the drain region and the second field plate includes a first portion spaced from a second portion by a second gap. *Id.* The third field plate includes a first portion spaced from a second portion by a third gap, and the first gap is wider than the second gap and the third gap, and the second gap is wider than the third gap. *Id.* The gaps are filled only with an insulation material and the first portion and the second portion of the second field plate, and the first portion and the second portion of the third field plate are disposed around the

drain region. *Id.* As noted in claim 1, the semiconductor device exhibits a breakdown voltage of at least 600 volts. *Id.*

As disclosed in the present application, in one embodiment, a field plate structure is formed over resurf region 30, where the field plate structure includes a first field plate having first portion 32 and second portion 33 spaced from its first portion 32 by gap 39, a second field plate having first portion 36 and second portion 38 spaced from first portion 36 by gap 40, and a third field plate having first portion 42 and second portion 44 which is spaced from first portion 42 by gap 46. *See, e.g.,* Figure 1 and related text of the present application.

As further disclosed in the present application, the first field plate structure is disposed over resurf region 30, which is formed in epitaxially formed semiconductor layer 12 between drain region 26 and body region 14 over at least a portion of drift region 28, where second portion 33 of the first field plate is electrically connected to drain region 26 by electrical connectors 50 and second portion 38 of the second field plate structure. *See, e.g., id.* at Figure 1 and related text. As disclosed in the present application, a field plate in accordance with the present invention can reduce the surface charge on the field insulation beneath each plate to advantageously permit the devices to withstand 650 V or more when applied in, for example, 0.35 micron CMOS. *See, e.g., id.* at paragraph [0012].

In the outstanding Office Action, the Examiner acknowledges that Fujishima does not disclose a resurf region of the first conductivity type in the semiconductor layer,

wherein the resurf region is formed over at least a portion of the drift region between the body region and the drain region, and wherein the drift region is adjacent to and in contact with the drain region. *See* item 5 of the outstanding Office Action. In an attempt to overcome the acknowledged deficiency in Fujishima, the Examiner suggests combining Figure 19 of Fujishima with Figure 10 of Tada. *Id.* Applicant submits that the combination of Fujishima and Tada cannot and does not result in the present invention as described in independent claim 1.

The Examiner alleges that it would be obvious to include "resurf region 44" in the device of Fujishima, the motivation being to secure certain breakdown voltage, to facilitate obtaining stable and reliable breakdown voltage, and to reduce on-resistance. *Id.* As disclosed in Tada, a conventional n-channel lateral power MOSFET includes highly resistive P type substrate 101, N type offset region 103 in the surface portion of P type substrate 101, P type base region 102 in the surface portion of P type substrate 101, N^+ type source region 105 in the surface portion of P type base region 102, N^+ type drain region 106 in the surface portion of N type offset region 103, and P type offset region 104 in the surface portion of N type offset region 103. *See, e.g.,* Figure 19 and column 1, lines 37-62 of Tada.

As disclosed in Tada, when high voltage is applied between the source and the drain of the lateral power MOSFET packaged in a plastic mold, especially at high temperatures, positive ions 115a and positive electric charges in the plastic mold are attracted toward source electrode 111, and negative ions 115b and negative electric

charges in the plastic mold are attracted toward drain electrode 112. As a result, in the portion to which the positive ions 115a and positive electric charges are attracted, protection film 114, interlayer film 113 and field oxide film 108 constitute a capacitor. On the substrate side thereof, negative electric charges 115c are induced, which turn a part of P type offset region 104 to an N type. In the portion to which negative ions 115b and negative electric charges are attracted, positive electric charges 115d are induced. The induced positive electric charges 115d thicken a portion of P type offset region 104.

Thus, the original P type offset region 104 deforms to P type offset region 104a causing an imbalance between the expanding depletion layers, a strong electric field locally, and lowers the breakdown voltage between the source and the drain. Furthermore, since P type offset region 104 is formed in the surface portion of N type offset region 103 to promote depletion at reverse bias voltage application, the main current path is pinched off easily as the drain voltage rises and, thereby, the on-resistance is increased. It will be appreciated that the above teaching of Tada is applicable to Fujishima, and would be especially pronounced at high voltages, for example at those around 600 volts or above. *See, e.g.,* Figure 19 and related text of Fujishima.

Thus, Tada teaches and discloses including spiral polysilicon thin film 10 arranged on field oxide film 8. *See, e.g.*, Figure 10 and column 10, lines 16-18 of Tada. An end of thin film 10 is connected to drain electrode 12 and another end thereof to source electrode 11. *Id.* As disclosed in Tada, by including spiral thin film 10, the local potential at a specific location on substrate 1 is almost equalized by the local potential at a specific

location, above the specific location on substrate 1, of spiral thin film 10, and a stable breakdown voltage is obtained. *See, e.g., id.* at column 10, lines 40-50. Moreover, since spiral thin film 10 exhibits shield effects against disturbances such as ions 15 (or electric charges) in the plastic mold of the semiconductor device, deviations of the breakdown voltage are hardly caused, even when high voltage is applied at a high temperature. *Id.* Thus, Applicant submits that the combination of Fujishima and Tada cannot disclose and rather teaches away from, for example, first, second, and third gaps, where the gaps are filled only with an insulation material as described in independent claim 1.

In the outstanding Office Action, the Examiner acknowledges that Fujishima does not disclose the first plate including a second portion spaced from the first portion of the first plate including a second portion spaced from the first portion of the first plate by a first gap wider than the second gap, wherein said second portion is electrically connected to the drain region. *See* Item 7 of the outstanding Office Action. In an attempt to overcome the acknowledged deficiency in Fujishima, the Examiner suggests combining the combination of Figure 19 of Fujishima and Figure 10 of Tada with Figures 1 and 2 of Rumennik. *Id.* However, Applicant submits that the combination of Fujishima, Tada, and Rumennik does not disclose or make obvious the present invention, as described in independent claim 1.

Rumennik discloses drain electrode 11 providing an electrical connection to N+ drain diffusion region 19, where drain electrode 11 also connects to field plate member 26, which is insulated from the substrate and is located adjacent to drain diffusion region

19 over N-well region 17. *See, e.g.*, Figure 1 and column 4, lines 37-45 of Rumennik. As described in Rumennik, field plate member 26 acts to reduce peaks in the localized electric field, thereby increasing the breakdown voltage of the transistor. *Id.* Thus, Rumennik discloses field plate member 26 over N-well region 17 in an n-channel device, similar to drain electrode 12 in Figure 19 of Fujishima, and does not teach or disclose field plate member 26 over a P type region at the top surface of the substrate as would be required by the combination of Fujishima with Tada as suggested by the Examiner.

Furthermore, assuming *ad arguendo*, that Fujishima, Tada, and Rumennik are combinable as suggested by the Examiner, none of the above art discloses a three field plate structure and nothing in the cited art would teach or suggest, for example, a first field plate including a first portion spaced from a second portion by a first gap, where the first gap is wider than the second gap and the third gap. More particularly, even if field plate member 26 of Rumennik is somehow combinable or should be combined with Fujishima and Tada, there is nothing to teach or suggest a first gap wider than second and third gaps.

Also, the field plates or similar structures in each of Fujishima, Tada, and Rumennik are carefully designed to manipulate electric fields and thus have particular structures and functions. Thus, it cannot be assumed that when combining the cited art, similar benefits can be obtained at all or at least without significantly altering the overall structure of a resultant device. For example, among other differences, each device is optimized and designed for different applications, have different doping profiles, and

different dimensional requirements, such as insulator thickness requirements. Thus, any change to one variable would ripple through the design and alter the structure, design, and performance of the entire device. For example Tada, as described above, is just one example illustrating the changes to a device that are required by altering the design of a semiconductor device. As another example, in the outstanding Office Action, the Examiner argues that the first thickness in Fujishima, as well as other thicknesses of different insulation layers, affects the performance and the area of the device and it is therefore necessary to ensure that the insulation layers are of an appropriate thickness. *See* item 15 of the outstanding Office action. However, the Examiner concurrently maintains that significantly different structures having different insulation layer thicknesses can simply and obviously be combined into a functional and practical device.

In contrast to the cited art, the present application is directed to the challenges faced as designers attempt to design high voltage semiconductor devices with smaller features. *See, e.g.*, paragraph [0006] of the present application. For example, in lateral conduction MOSFETs, as photolithography line width is decreased, field oxide thickness also decreases. *Id.* As a result, for example, in 0.35 micron CMOS technology, the initial breakdown voltage of high voltage (600 volts and higher) devices with conventional multiple floating field plate ("MFETP") structures is decreased to below 600 volts because of the high electric field concentration on the oxides under the field plates, which is due to the reduction in the thickness of the field oxide. *Id.* In light of the foregoing, and in light of additional limitations the Examiner acknowledges are not disclosed in

Fujishima, Tada, and Rumennik, Applicant respectfully requests that the Examiner reconsider the rejection of independent claim 1.

For the foregoing reasons, Applicant respectfully submits that at the time the invention defined by independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art in light of the teachings provided by Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan, either individually or taken in combination. Thus, Applicant respectfully asserts that independent claim 1 is patentably distinguishable over Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan and, as such, claims 2-7, 9, 11, 13, and 20-23 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Fujishima, Tada, Rumennik, Van Zant, Ghandhi, Noda, and Ranjan for at least the reasons presented above, and also for the additional limitations contained in each dependent claim.

B. Rejection of Claims 30-35 under 35 USC §103(a)

The Examiner has rejected claims 30-35 under 35 USC §103(a) as being unpatentable over United States Patent Number 4,766,474 to Nakagawa et al. (hereinafter "Nakagawa") in view of United States Patent Number 6,492,679 B1 to Imam et al. (hereinafter "Imam"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 30, is patentably distinguishable over Nakagawa and Imam, either singly or in combination.

In contrast to the present invention, as described by amended independent claim 30, Nakagawa and Imam do not disclose a field plate structure including a first field plate having a first portion and a second portion separated by a first gap, where the first field plate is disposed over a first insulation layer on top of a reduced surface field drift region of the laterally diffused high voltage device, and a second field plate having a first portion and a second portion, the first portion of the second field plate electrically connected to the first portion of the first field plate, the first portion and the second portion separated by a second gap, where the second field plate is disposed over the first field plate by a second insulation layer, and where the second gap is narrower than the first gap.

Applicant has amended independent claim 30 to provide that the first portion of the second field plate is electrically connected to the first portion of the first field plate, which is not taught or disclosed by Nakagawa or Imam. For example, Nakagawa discloses a MOS transistor including first and second covering layers having covering elements for covering a channel region of the semiconductor device, and a field plate layer, as a third covering layer disposed over the first and second covering layers. *See, e.g.*, Figure 2(f) and the abstract of Nakagawa. As disclosed in Nakagawa, field plates 8' and 9' are disposed on third insulating layer 15 while each of field plates 8' and 9' extend from each of source electrode 8 and drain electrode 9 respectively. *See, e.g., id.* at column 2, line 67 through column 3. Source electrode 8 is connected to N^+ type source region 2 and drain electrode 9 is coupled to N^+ type drain region 3. *See, e.g., id.* at

column 2, lines 48-50. Thus Applicant submits that Nakagawa and Imam fail to make obvious the present invention, as described in amended independent claim 30.

For the foregoing reasons, Applicant respectfully submits that at the time the invention defined by amended independent claim 30 was made, the invention would not have been obvious to a person of ordinary skill in the art in light of the disclosures provided by Nakagawa and Imam, either singly or in any combination. Thus, Applicant respectfully asserts that amended independent claim 30 is patentably distinguishable over Nakagawa and Imam and, as such, claims 31-35 depending from amended independent claim 30 are, *a fortiori*, also patentably distinguishable over Nakagawa and Imam for at least the reasons presented above, and also for the additional limitations contained in each dependent claim.

C. Conclusion

For all the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 30, and claims depending therefrom, I patentably novel and inventive. Accordingly, an early allowance of claims 1-7, 9, 11, 13, 20-23, and 30-35 pending in the present application is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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Respectfully Submitted,
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